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EXAMINER	
MONDT, JOHANNES P	
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3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,104	OGIHARA ET AL.	
	Examiner	Art Unit	
	JOHANNES MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5,6,9,10,18,20,37 and 39-42* is/are pending in the application.

4a) Of the above claim(s) *42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5,6,9,10,18,20,37 and 39-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed 03/03/2009 forms the basis for this Office action. In said Amendment applicants substantially amended all pending claims and added new claims 40-42. Comments on "Remarks" submitted with said Amendment are included below under "Response to Arguments".

Election/Restrictions

2. Newly submitted claim 42 is directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the claim listing contains the following groups drawn to different inventions:

- Invention I: Claims 5, 6, 9, 10, 20, 37 and 39, drawn to an apparatus, classified in class 257, subclass 499+.
- Invention II: Claim 42, drawn to a method of fabricating an apparatus, classified in class 438, subclass 400+.

The inventions are distinct, each from the other because of the following reasons:

3. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process, for instance one in which disposing each semiconductor thin film over the metal layer occurs not after forming said each

semiconductor thin film, but instead occurs during the formation of said semiconductor thin film, e.g., by chemical or physical vapor deposition technology..

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 42 is herewith withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Accordingly, claims 5, 6, 9, 10, 20, 37 and 39 have been examined.

Specification

The following is a quotation of 35 U.S.C. 132 (a):

> Whenever, on examination, any claim for a patent is rejected, or any objection or requirement made, the Director shall notify the applicant thereof, stating the reasons for such rejection, or objection or requirement, together with such information and references as may be useful in judging of the propriety of continuing the prosecution of his application; and if after receiving such notice, the applicant persists in his claim for a patent, with or without amendment, the application shall be reexamined. No amendment shall introduce new matter into the disclosure of the invention.

1. The Amendment to the Specification is, once again, objected to for the introduction of new matter: the limitation *"inorganic compound"*, newly introduced by amendment on page 11, line 7, constitutes new matter, because although the examples of "other materials" as previously disclosed are inorganic semiconductor materials, these materials have not been disclosed to be compounds, and in fact they are not (see, e.g., "The Columbia Encyclopedia", Columbia University Press 2004 for the definition of "chemical compound"). Furthermore, it is noted that although original claim 16 now canceled recited said semiconductor thin film to be a compound semiconductor

material, it did not claim said semiconductor thin film to be an *inorganic* compound. Applicant is required to cancel the new matter in any responsive reply to this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39-41*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly introduced limitation "said semiconductor thin film being made of an inorganic compound semiconductor as a main material" (lines 15-17 of claim 5) does not find support in the specification as originally filed. The reasons for this rejection are the same as the reasons for the objection to the Specification under 35 USC 132(a) (see section 3 above).

4. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39-41*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation "small enough to include a single light-

emitting element" implies logically that there be a size range with zero as limit point, in which the claimed "each semiconductor thin film" may include a single light-emitting element. However, given any light-emitting element such a size range clearly is a logical impossibility, because a finite size is required to accommodate said light-emitting element. Considering the breadth of the claims with regard to the disclosed light-emitting element and semiconductor thin films, the nature of the invention, which is limited anyway to the conventional, as opposed to the nano-scale, device technology, the state of the prior art, in which any light-emitting element requires a finite size, the level of ordinary skill in the art, which level is such that one of ordinary skill would not know how to accommodate a light-emitting element of the aforementioned conventional art, in a semiconductor thin film of arbitrarily small size, the level of predictability in the art, which breaks down within said conventional art, at the scale in which quantum wave functions overlap with the edges of the thin film (i.e., nano-size), and the absence of any working examples and direction by inventor for extrapolating to arbitrarily small sized thin films, it is concluded that the quantity of experimentation needed to make or use the invention based on the content of the disclosure and as defined by claim 5 amounts to undue experimentation as requirement to practice the invention. See MPEP 2164.01(a).

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39-41*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The lack of support

noted above in section 5 above for the newly introduced limitation "said semiconductor thin film being made of an inorganic compound semiconductor as a main material" (lines 15-17 of claim 5) in the specification renders the metes and bounds of said limitation vague and ill-defined, causing the claims to be indefinite.

7. ***Claims 5, 6, 9, 10, 18, 20, 37 and 39-41*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The lack of enablement noted above in section 6 above renders the metes and bounds of said limitation vague and ill-defined, causing the claims to be indefinite.

8. ***Claims 5, 6, 7, 9, 10, 18, 20, 37 and 39-41*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the limitation "other process" (claim 5, lines 10-11) is vague and ill-defined because the limitation introduces a process with the exclusion of an undefined process in relation to which said process has to differ. The collection of processes from which any practitioner of the invention is to choose is thus ill-defined and vague, rendering the claims indefinite.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. ***Claims 5, 37 and 40-41*** are rejected under 35 U.S.C. 103(a) as obvious over Kub et al (US 6,242,324 B1) (as cited previously), relying for evidence on M. Fukuda ("Optical Semiconductor Devices", Wiley Series in Microwave and Optical Engineering, Kai Chang, Series Editor, John Wiley & Sons, Inc., New York, 1999; page 211). N.B.: The rejection is provided subject to the noted indefiniteness under 35 USC 112, 2nd par., as detailed above (sections 7-10), to the best of examiner's understanding, interpreting the process limitation "other [process" to be solely a process limitation regardless its exact scope, and assuming the limitation for the semiconductor thin film as being "small enough to include" to mean "sized to be capable of including" (a light-emitting element).

Kub et al teach a combined semiconductor apparatus (see title and first sentence of abstract; see Figures 3 and 5, col. 9, l. 36 – col. 11, l. 18), comprising: a silicon substrate 12 having a CMOS integrated circuit formed therein ("CMOS" = complementary metal on silicon) (col. 9, l. 36), the silicon substrate having a rough or irregular surface due to at least a wiring pattern of the integrated circuit (the wiring is the interconnect structure 36 or 68: see col. 9, l. 2-13 , col. 11, l. 16+, and Figures 3 and 5);

a planarized region 22 (col. 9, l. 36-38; Figure 3) defined over said rough or irregular surface of said silicon substrate in Figure 3, while although oxide region 56 in Figure 5 is not expressly referred to as planarized, it would at least have been obvious to try since layer 56 is introduced in Kub et al as "the" oxide layer 56, antecedent basis only being available through the previous embodiments, which all feature a planarized

oxide layer (such as 22 in Figure 3) at the same relative position to other layers, while the same technology (CVD followed by CMP (col. 9, l. 3-5) as employed for layer 22 can be applied with reasonable expectation of success, which renders "planarized" for region 56 in Figure 5 obvious (see MPEP 2141) (N.B.: the embodiment of Figure 5 is characterized as "similar" to that of Figure 2 (col. 10, l. 49-52) wherein the layer similar to 56, i.e., layer 22 is planarized (col. 9, l. 3-5));

a substantially planar metal layer 38 or 54 (col. 9, l. 38-39, col. 10, l. 66- col. 11, l. 9) disposed over said planarized region (Figures 3 and 5); and

at least one semiconductor thin film 40 or 50/58 (col. 9, l. 63+, col. 10, l. 66+), or, in alternative interpretation 40/44/46 or 50/58/64/66 (N.B.: CdTe is an inorganic compound semiconductor) disposed over said metal layer and suitably sized to be *capable* of including a single light emitting element (CdTe/HgCdTe material layers 44/46 or similar material layers 64/66 of photo-detectors in Figure 5: see col. 9, l. 65+ and col. 11, l. 13+, respectively are p/n diodes, which, as has long been known in the art to be capable of being used as light-emitting elements such as much as photodetectors, see Fukuda, page 211)) and being wafer bonded (col. 9, l. 64) on grown on top of said metal layer (through layer 42 in the case of layer 40) and disposed over the integrated circuit (Figures 3 and 5) and said metal layer electrically connects said optoelectronic element to said integrated circuit (col. 9, l. 38 - col. 10, l. 13). Applicant is reminded that the limitation "to be small enough to include a single light-emitting element" is a limitation of intended use, and as such must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from

the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the instant case, the p/n diode 44/46 can be used as light-emitting diode just as readily as its use as a photodiode, as witnessed by Fukuda, and hence it is concluded that the prior art meets the claim limitation.

Furthermore, and even arguendo, although the illustrated and detailed embodiments by Kub et al are drawn to the photo-detector art, Kub et al expressly state that "other semiconductor thin film crystal layers" such as "GaAs" and "InP" can be bonded to the metal layer for making a light-emitting diode (LED) (see col. 10, l. 29-46) (GaAs and InP are both inorganic compounds). The limitation "light-emitting element" is thus obvious over Kub et al itself, in particular their suggestion to use the approach described in the detailed description also to the art of LEDs. *Motivation* for including said suggestion derives from the profit advantage of maximizing the range of applicability of the invention along the suggestion of its inventors.

On claim 37: additionally, Kub et al teach with respect to the embodiment of Figure 3 that a thin oxide layer 42 may be used (optionally) to cover the metal layer (col. 9, l. 42-62), but that in any case it is "likely necessary" that the surface of the resulting structure be CMP polished to small surface roughness (which implies "planarized") (loc.cit.). In the presence of 42 this implies that the metal layer and the inter-dielectric layer 42 form a planarized film. With regard to the limitation "the same thickness" applicant is further reminded that it has been held that Applicant's disclosure does not teach why the range as claimed is critical to the invention. In view of the absence of a

teaching why a range is critical to the invention Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

On claim 40: Kub et al disclose inter alia GaAs as main material for their apparatus (see, for instance, col. 4, l. 4-7, col. 10, l. 29+, and their claim 24).

On claim 41: metal layer 54 is in direct contact with 50 and hence with semiconductor thin film 50/58/64/66.

10. ***Claims 9, 10 and 18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of either Walsh (US 6,351,327 B1) or Tohyama et al (US 6,433,367 B1). As detailed above, claim 5 is unpatentable over Kub et al. Kub et al do not necessarily teach the further limitation as defined by claim 9; however it would have been obvious to include said further limitation in view of Walsh, who, in art on the application of CMOS technology to integrated LED driver and LEDs (67 and 69-71, resp.) (col. 3, l. 9-24), teach the application of a common electrode layer 33 (col. 4, l. 6-15) on a surface of a semiconductor thin film 39 (loc.cit.) opposite to the surface on which the light-emitting element (69-71) is formed. See Figures 1 and 2). The application of the teaching of a common electrode when included in the invention by Kub et al meets the claim limitations and would have been obvious as only one common reference voltage is needed to drive the LEDs. *Motivation* stems from economy of construction.

Similarly, Tohyama et al disclose an LEDs 13 with common electrode 17 (Figure 1 and col. 2, l. 55 - col. 3, l. 34) in integrated circuitry on the second surface 10e of the LED chip array. The application of the teaching of a common electrode when included in the invention by Kub et al meets the claim limitations and would have been obvious as only one common reference voltage is needed to drive the LEDs. *Motivation* stems from economy of construction.

On claim 10: said integrated circuit includes individual electrode terminals 36 or 68 (see Figures 3 and 5; col. 9, l. 12-14 and col. 11, l. 10-18 in Kub et al); and said apparatus comprises individual interconnecting lines formed on a region extending from an upper surface of said light-emitting element to said individual electrode terminals (see top portion of Figures 3 and 5; loc.cit. in Kub et al).

On claim 18: in the combined invention as defined above, said light-emitting element is a plurality of light-emitting elements arranged in said semiconductor thin film.

11. ***Claim 20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of Tohyama et al (US 6,433,367 B1).

Although Kub et al do not necessarily teach the further limitation defined by claim 20, the application of optical printer head would have been obvious over Tohyama et al, who, in a patent on an LED array chip (title, abstract and col. 2, l. 55 – col. 3, l. 34), hence art analogous to Kub et al, teach the application to an optical printer head (col. 3, l. 23-34 and their claim 11). *Motivation* to include the teaching by Tohyama et al in this regard is the obvious advantage to apply a device to a function when it is demonstrably capable of performing the function.

12. ***Claims 39 and 6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kub et al as applied to claim 5 above, and further in view of Ferra et al (US 2002/0155795 A1). As detailed above, claim 5 is unpatentable over Kub et al. Kub et al do not teach the further limitations by claim 39 and 6. However, it would have been obvious to include said limitations in view of Ferra et al, who, in a patent application drawn to the use of a CMP tool for planarizing layers (title, abstract), hence analogous to the planarization aspects in Kug et al, teach (1) the inclusion of a metal barrier layer between metal lines 101 on the one hand and an underlying wafer 100 and neighboring dielectric 103 on the other hand, so as to prevent the metal in the metal layer from migrating into a neighboring dielectric (see [0036]), and (2) the planarization of both barrier layer and metal layer ([0036]-[0039]). Hence said barrier layer 102 meets the limitation planarized film, while, when implemented in the invention by Kug et al said planarized film is disposed on a planarized region, wherein said metal layer is disposed on said planarized film. With regard to claim 6, said planarized film 102 is an interdielectric film. Motivation to include the barrier film in Kug et al derives from the resulting advantage of the prevention of migration of metal into the dielectric planarized region (CVD oxide 22 in Kug et al) as taught by Ferra et al. The inclusion of the teaching on planarizing both barrier and metal layers would at least have been obvious because the technique for improving a particular class of devices was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

Response to Arguments

5. Applicant's arguments filed 3/3/09 have been fully considered but they are not persuasive.

a. Applicant's allegation that the materials $(Al_xGa_{1-x})_yIn_{1-y}P$ are all compounds (pages 7-9) appears to rest at most on an allegation in the wholly un-refereed internet literature, in particular Wikipedia. This is not an authoritative, refereed source. Examiner, in contrast, referred in the previous Office action, to the authoritative Columbia Encyclopedia (Columbia University Press, 2004), and could well have referred to college or high-school text books on this matter. In response to applicant's calculation of ratios, said calculations are performed with a lumping of atoms of the same valence, while it is noted that the implication of the claim language is that materials other than GaN are compounds, of which claim 40 provides newly submitted additional evidence. Said reference suffices, however, and applicant's argument in this regard fails to persuade for the above reason.

b. Applicant's allegation that "inorganic" does not introduce new matter (page 10) appears based on the disclosure of some inorganic materials. However, as such, "inorganic" constitutes a broadening not supported by the specification, and hence as such constitutes matter. Therefore, applicant's argument fails to persuade.

c. Applicant's allegation of patentability of claims 5 and 37 (page 11 of Remarks) appears to be based on the inclusion of the limitation that the

semiconductor thin film is "made other process". Applicant is reminded that this limitation is a product-by-process limitation. The limitation is only of patentable weight in as much as the method step distinguishes the final structure, and to the extent not impacting final structure is taken to be a product-by-process limitation and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not. Applicant does not show any structural distinction flowing from the specific product-by-process limitation. Moreover, "made from other process" implies a pointer to a "process", without which the adjective "other" is meaningless, vague and ill-defined. The claims are thereby rendered indefinite under 35 U.S.C. 112, 2nd paragraph. Finally, the newly added limitation "small enough to include" is logically deficient: given what needs to be included, the structure within which another structure needs to be included has a size that is bounded from below, not from above. Therefore, the claims are not enabled, and are also indefinite for not being enabled. Yet furthermore, applicant's traverse on the merits of the rejection over Kub is also deficient

because the specific embodiment cited in the office action has a photo-detector diode included in e.g. 40/44/46 (see Office action, page 6, second line from below), which, in contrast to applicant's allegation on page 13 of Remarks, is an active solid-state device, while Kub et al is explicit in including as alternative embodiments not only photodetectors but also light emitting devices (see Kub, e.g., abstract and col. 1, l. 11+); while the currently amended claim language does not even positively recite any light-emitting element, but only requires each semiconductor thin film to be able to include a single light-emitting element. The claim limitation "to be small enough to include...to said integrated circuit" is only a limitation of intended use, because the light-emitting element is not positively recited. Applicant is reminded that Applicant is reminded that intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). The instant size limitation for the semiconductor thin film is met because, as has been known for decades, the difference between photo-detector and light-emitting devices in the semiconductor art is not one of semiconductor diode structure or size but only a matter of the application to the diode of either light (photo-detector application) or electrical voltage (light-emitter application). See, for instance, M. Fukuda, page 211, introduction. Therefore, the prior art structure is capable of performing the

intended use. With regard to applicant's argument that Kub does not disclose semiconductor thin film based on the method of its manufacture (page 13): as mentioned above, the limitation "other process" is not only vague and ill-defined, but also one of product-by-process and as such does not distinguish over the prior art structure. Again, on page 13, central paragraph, applicant attempts to distinguish based on the process by which the apparatus is made, which does not persuade, with reference to the above comments on product-by-process. No other arguments are presented that are independent of the ones discussed overhead. The newly added claims are being examined for the first, and at the earliest possible, time.

For the above reasons applicant's argument in traverse of the art rejections of record in the previous Office action fail to persuade.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 8-17.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOHANNES MONDT/
Primary Examiner, Art Unit 3663